REMARKS

Claims 1-23, 25, 26, and 28-38 are pending. In this paper, new claim 38 has been added to recite additional features of the embodiments disclosed in the specification. Also, in this paper the proper status identifier has been provided for claim 5 in response to the Notice of Non-Compliant Amendment.

In the Office Action, claims 1-30 were rejected under 35 USC § 102(e) for being anticipated by the Dally publication. This rejection is traversed for the following reasons.

Claim 1 recites a clock generator which generates a number of clock signals to control sampling of a data stream. The clock signals are generated to have equally spaced phases, where the equally spaced phases are "determined by a predetermined fraction of a data rate frequency of a data stream." The Dally publication does not disclose these features.

The Dally publication discloses a plurality of samplers that sample data based on clock signals having equally spaced phases. However, the Dally publication does not disclose that the equally spaced phases of the clock signals are determined by a predetermined fraction of a data rate frequency of the input data stream.

The Examiner relied on the disclosure at Paragraphs [0008]-[0012]. Here, the Dally publication discloses that a phase interpolator 24 generates clock signals having equally spaced phases based on a reference clock and a phase setting 25 output from the divide-by-2P counter. The reference clock does not provide an indication of the data rate frequency of the data stream, and neither does phase setting 25.

Phase setting 25 is derived from the output of the early/late logic circuit 26. This circuit determines whether sample points output from samplers 22 are early or late relative to the data signal edges. Whether or not these edges are early or late does not provide an indication of the data rate frequency of the data stream. Rather, it indicates whether the

samples are in or out of phase with the data stream.

The output of the early/late logic circuit is divided by a factor N in filter 28, and then phase counter 29 counts the number of early or late samples. The phase setting 25 input into phase interpolator 24, therefore, determines the equal phase spacing of the clock signals based on the number of early or late samples, which also provides no indication of the data rate frequency of the input data stream. Rather, like the output of early/late logic circuit 26, phase setting 25 provides an indication of how the samples output from samplers 22 are out of phase with the input data signal.

The Examiner also cited two additional portions of the Dally publication to reject claim 1, namely Paragraphs [0019]-[0023] and [0069]-[0080]. However, these portions of Dally are similar to the disclosure in Paragraphs [0008]-[0012] in relation to how clock signals are generated with equally spaced phases, i.e., these clock signals are generated based on the output of an early/late logic circuit.

Because the Dally publication does not disclose sampling an input data stream based on clock signals with equally spaced phases that are "determined by a predetermined fraction of a data rate frequency of a data stream," the Dally publication does not anticipate claim 1 or any of its dependent claims.

Dependent claim 5 recites that each sampler "samples the data stream based on a different pair of the clock signals." The Dally publication does not disclose or suggest these features. In fact, the Dally publication teaches away from these features of the invention when it discloses that each sampler 22 samples input data based on one and only one clock signal. (See Paragraph [0012]: "The phase interpolator 24 generates **a** sample clock for **each** of the four samplers 22.") Claim 5 is therefore allowable, not only by virtue of its dependency from claim 1 but also based on the features separately recited therein.

Dependent claim 7 recites that "the number of samplers and the number of clock signal phases generated by the clock generator are different." The Dally publication does not disclose these features. Dally discloses that phase interpolator 24 generates four clock signals, one for each sampler 22. Accordingly, the number of samplers and the number of clock signal phases in Dally are the same, not different as required by claim 7. Applicants submit that claim 7 is allowable for these reasons and based on its dependency from claim 1.

Dependent claim 8 recites that each sampler samples the data stream "based on a different pair of clock signals having consecutive phases." The Dally publication does not disclose these features, i.e., Dally discloses generating one clock signal for each sampler, not different pairs of clock signals having consecutive phases for respective ones of the data samplers as required by claim 8. Accordingly, it is submitted that claim 8 is allowable.

Dependent claim 9 recites that the equal spacing of the clock signal phases corresponds to "a symbol duration of the data stream." The Dally publication does not disclose or suggest these features. Moreover, the Examiner failed to provide any indication in the Office Action of where these features may be found in Dally. Based on these omissions, it is respectfully submitted that claim 9 is allowable.

Claim 12 recites features similar to those which patentably distinguish claim 1 from the Dally publication. For example, claim 12 recites generating a number of clock signals having equally spaced phases, where each of the phases are "determined by a predetermined fraction of a data rate frequency of a data stream." The Dally publication does not disclose these features.

Claim 23 recites a sampling stage to sample data based on clock signals having different phases, wherein "the difference between the phases of the clock signals at least substantially equals a symbol duration of the data."

The Dally publication discloses generating clock signals having equally spaced phases. Dally also discloses determining whether samples are early or late relative to the input data signal. However, the Dally publication does not disclose or suggest that "the difference between the phases of the clock signals at least substantially equals a symbol duration of the data." Based on these differences, it is respectfully submitted that claim 23 is allowable.

Claim 26 recites features similar to those which patentably distinguish claim 23 from the Dally publication. Applicants therefore submit that claim 26 and its dependent claims are also allowable.

Claim 29 recites a clock generator to generate a number of clock signals having equally spaced phases "determined by a predetermined fraction of a data rate frequency of a data stream." The Dally publication does not disclose these features. Applicants therefore submit that claim 29 and its dependent claim are allowable.

Claim 31 recites that the samplers in claim 4 sample the data stream "based on sampling signals that are generated by different pairs of the clock signals." (See, for example, Figures 1-4 for support). The Dally publication does not disclose these features.

Claim 32 recites that consecutive pairs of the clock signals "share a common clock signal." (See, for example, Figures 1-4 for support). The Dally publication does not disclose these features.

Claim 33 recites that "the clock signals in each pair have consecutive phases." (See, for example, Figures 1-4 for support). The Dally publication does not disclose these features.

Claim 34 recites that "the sampling signals having non-overlapping duty cycles." (See, for example, pages 6 and 7 of the specification with reference to Figure 3). The Dally publication does not disclose these features.

Claim 35 recites that "the sampling signals have overlapping duty cycles." (See, for example, page 7 of the specification with reference to Figure 4). The Dally publication does not disclose these features.

Claim 36 recites that "the clock signals in each pair define different edges of corresponding ones of the sampling signals." (See, for example, Figures 1-4 for support). The Dally publication does not disclose these features.

Claim 37 recites that "the sampling signals have duty cycles which are substantially different from 50%." (See, for example, page 7 for support). The Dally publication does not disclose these features.

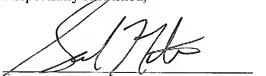
Claims 10, 11, 21, and 22 were rejected under 35 USC § 103(a) based on the Dally publication. Applicants traverse this rejection on grounds that the Dally publication does not teach or suggest all the features in base claims 1 and 12. Accordingly, claims 10, 11, 21, and 22 are allowable.

New claim 38 recites that "the sampling unit includes a plurality of samplers which sample the data stream based on different pairs of the clock signals that have consecutive overlapping phases." (See, for example, page 6 of the specification for support). These features are not disclosed in the Dally publication. Accordingly, it is submitted that claim 38 is allowable.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and timely allowance of the application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with this application to Deposit Account No. 16-0607 and credit any excess fees to the same Deposit Account.

Respectfully submitted,



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